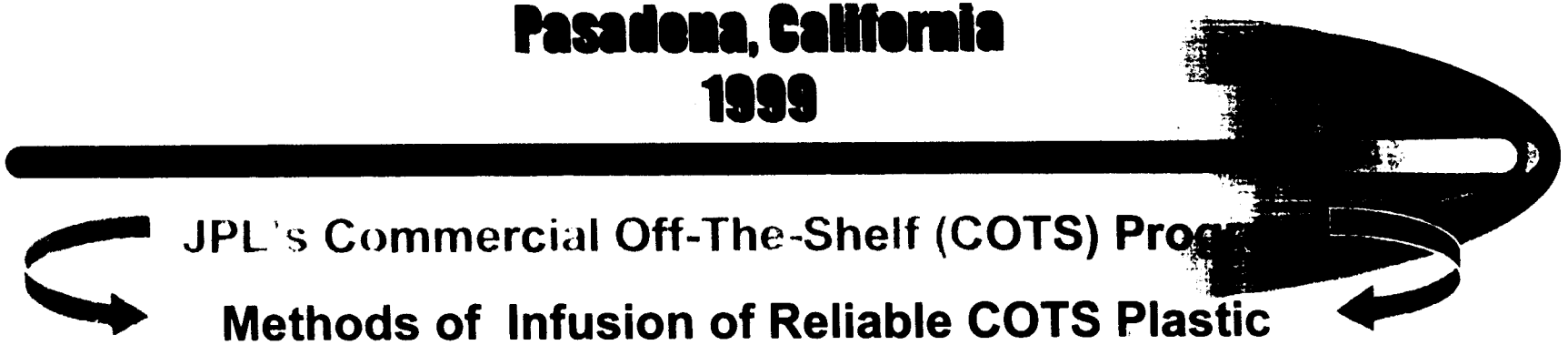
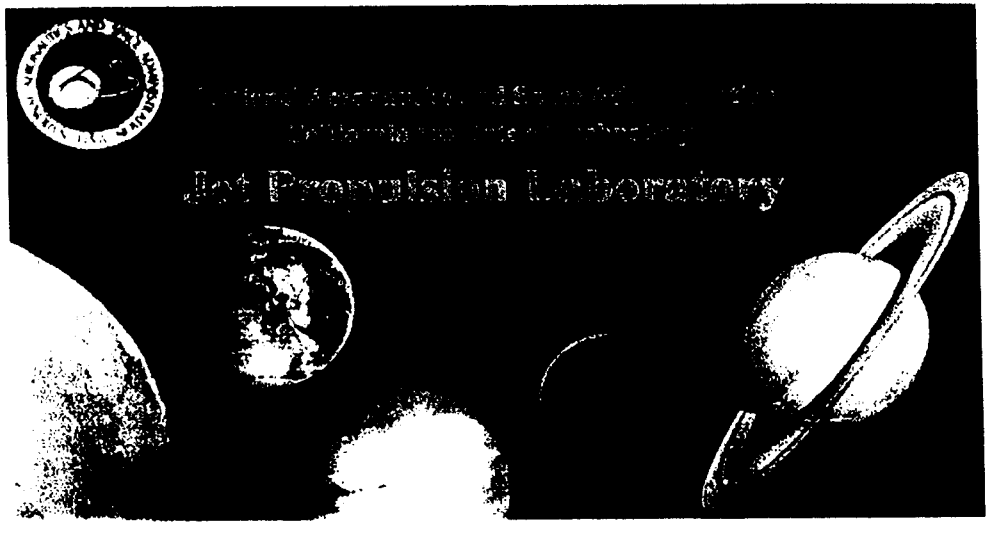
Microelectronics Reliability & Qualification Workshop
Pasadena, California
1999



JPL's Commercial Off-The-Shelf (COTS) Prog

Methods of Infusion of Reliable COTS Plastic Parts in NASA Flight Hardware



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Assessment Options for COTS Plastic Parts & Their Relativ

• Temperature/ Humidity	→	Corrosion	($)
• Temperature Cycling	→	Assembly Defects	($$)
• Moisture Absorption	→	Popcorning	($$)
• Radiation	→	TID Degradation	($$$$)
• Outgassing	→	Condensables	($)
• Glass Transition	→	Epoxy Stability	($$)
• Delamination	→	Voids/Stresses	($)
• Upscreening/Burn-in	→	Performance/Reliability	($$$$)
• DPA	→	Manufacturing Quality	($$)

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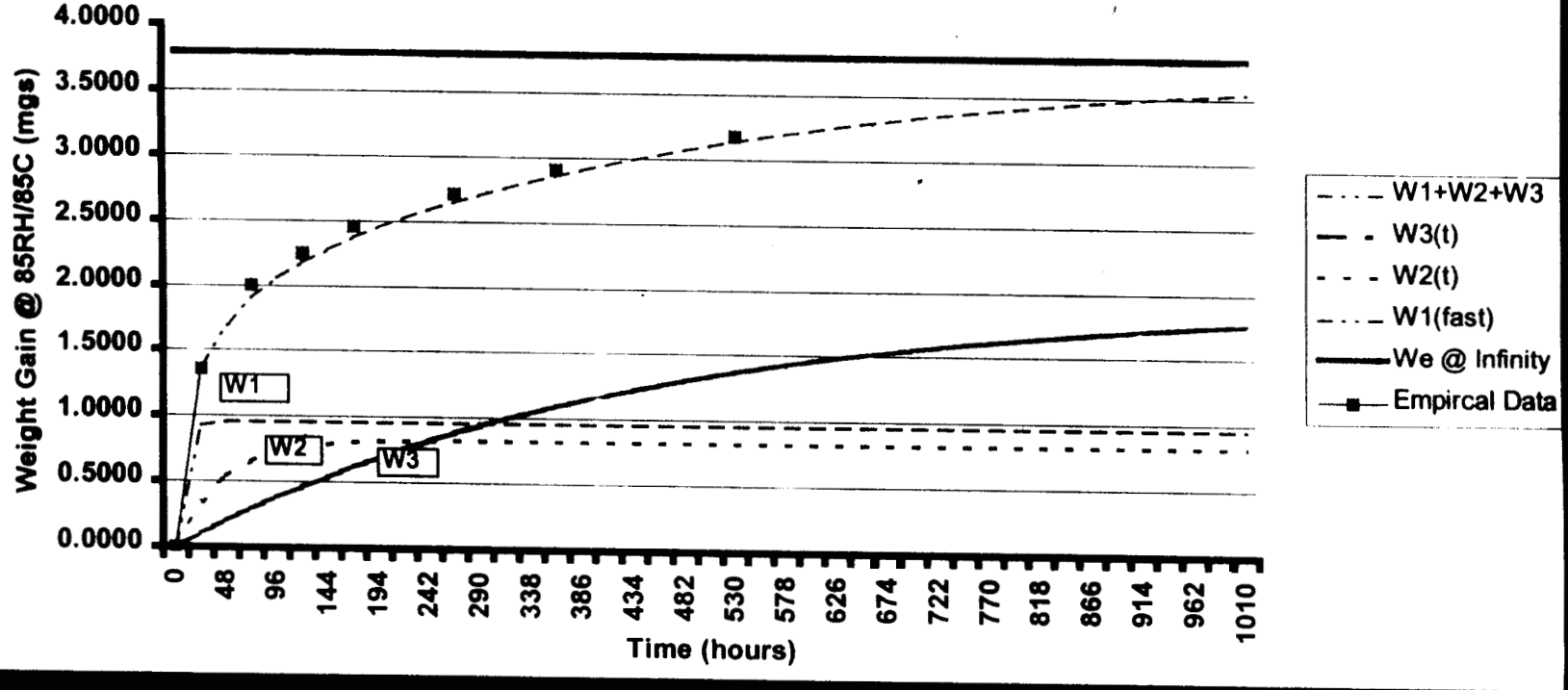
Moisture Multiple Absorption Model for SCR265 (Plastic)

$$W(t)=We(1-e^{-kt})$$



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Radiation Results on Plastic Parts

Moisture Absorption / Bake for Intel DA28F016SV in Plastic Package

(0.6 μm ETOX IV Process Technology)

Conditions: Test Temperature = 25°C, Vdd = 5.0V, Vpp = 5.0V

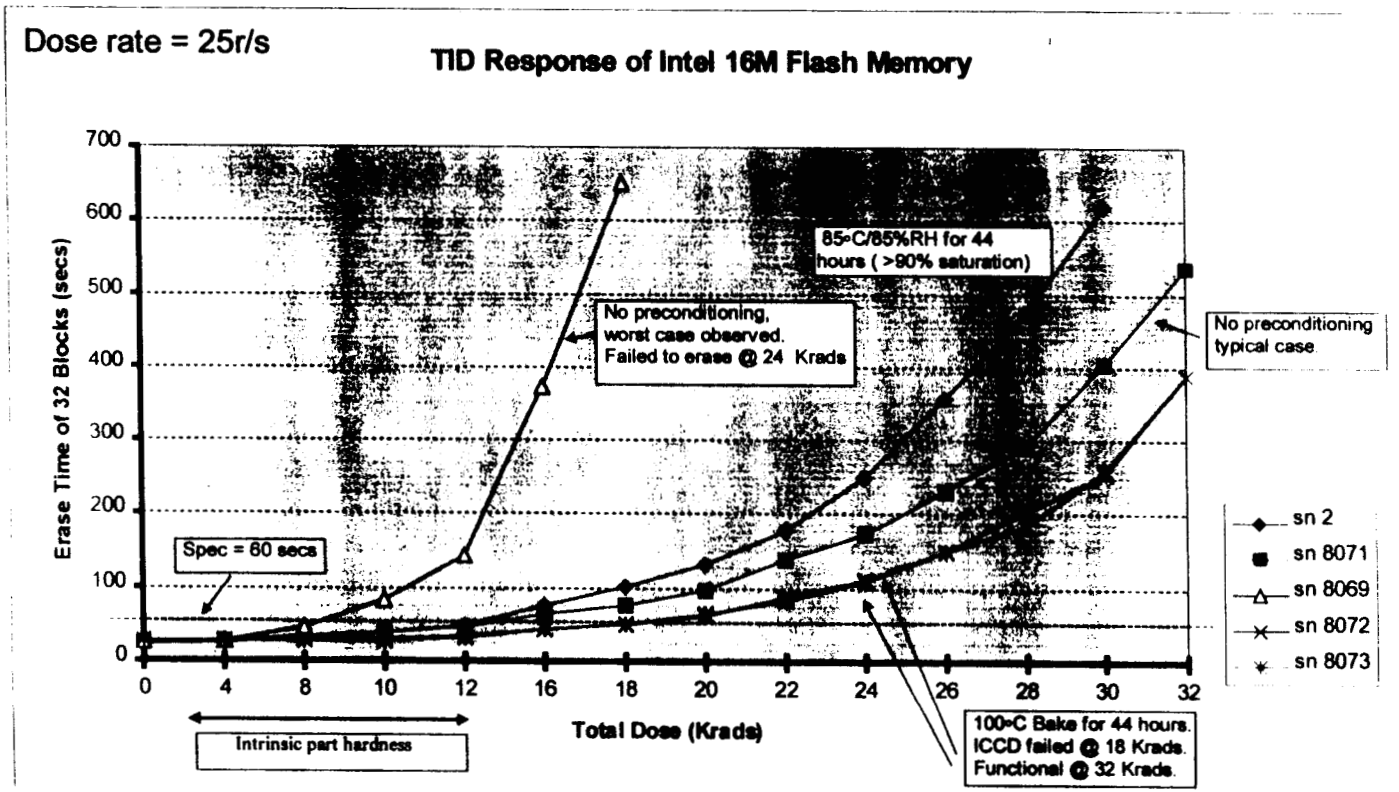

Figure 1
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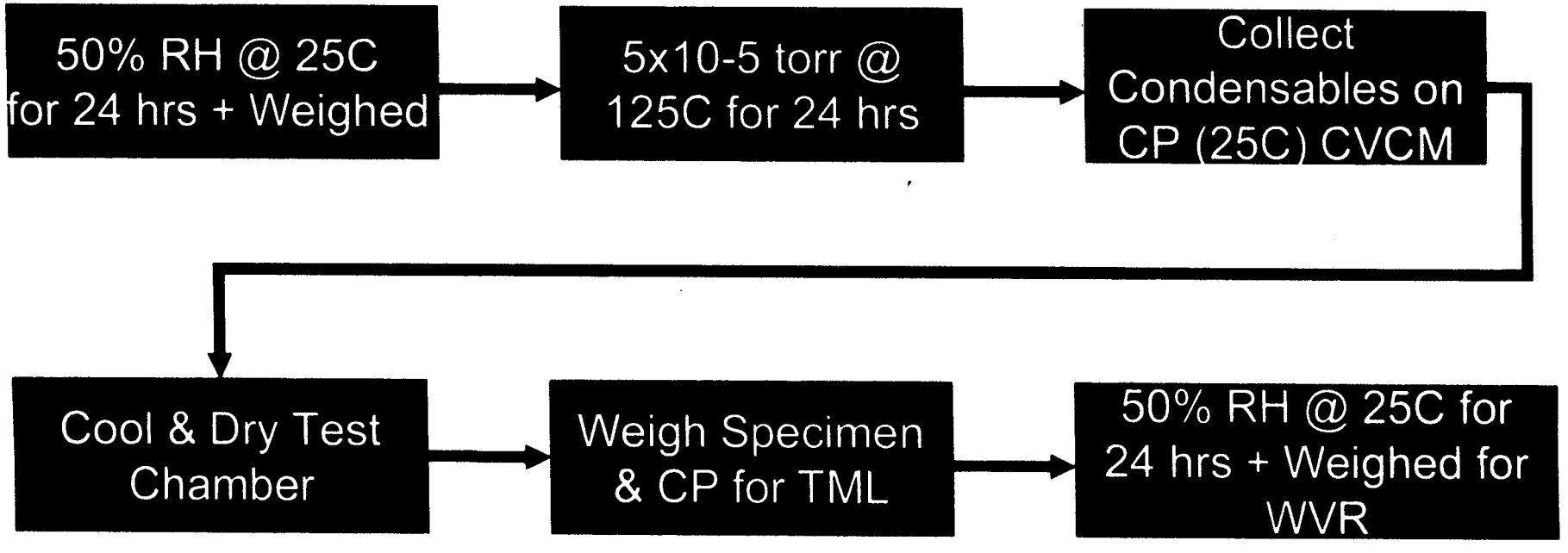
Outgassing Test Flow for Plastic Packages



Ref: ASTM E595-93

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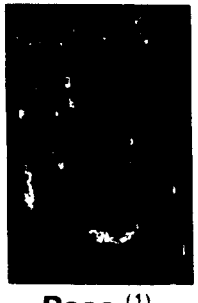
C-SAM Results (No. of Rejects):

Amplifier - Vendor A

Top Side: 0/78(1)

Back Side: 3/78

Typical Rejects:



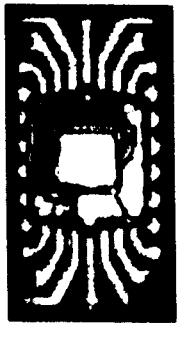
Pass (1)

Fail

ADC - Vendor B

Top Side: 30/78

Back Side: 8/78



Fail

Fail

DC-DC Converter - Vendor C

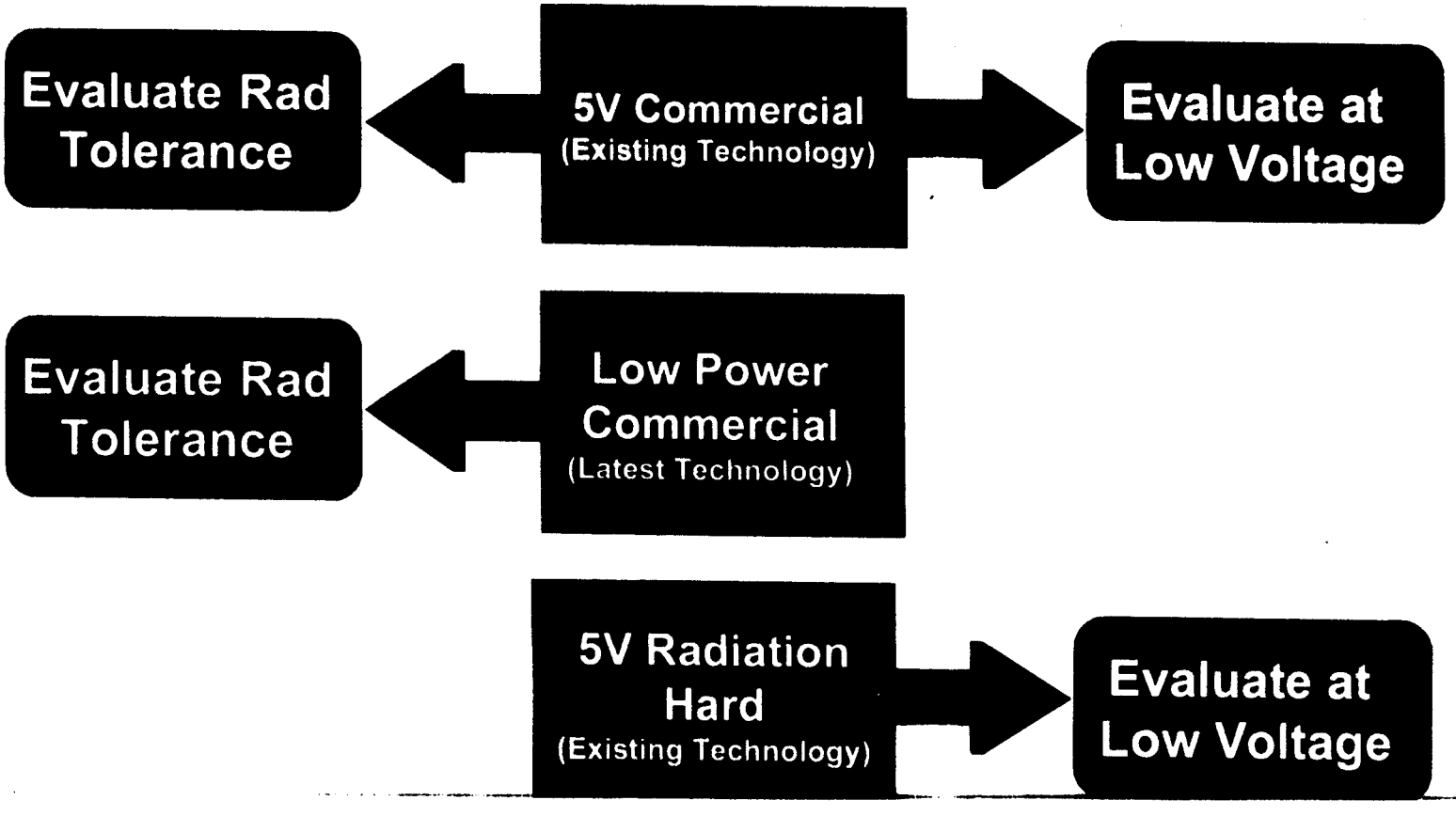
Top Side: 0/78

Thru Scan: 16/78

Fail

Note: Units with delamination are defective and were defined by JPL to be a potential risk to mission success. (1) All units showed 100% delaminationcaused by a special die top coating These parts were not rejected. F.A .confirmed a die top coating. This was validated by the supplier as a gel coat and is used to relieve stress of the die and improve performance.

Methods to Achieve Low Power Parts



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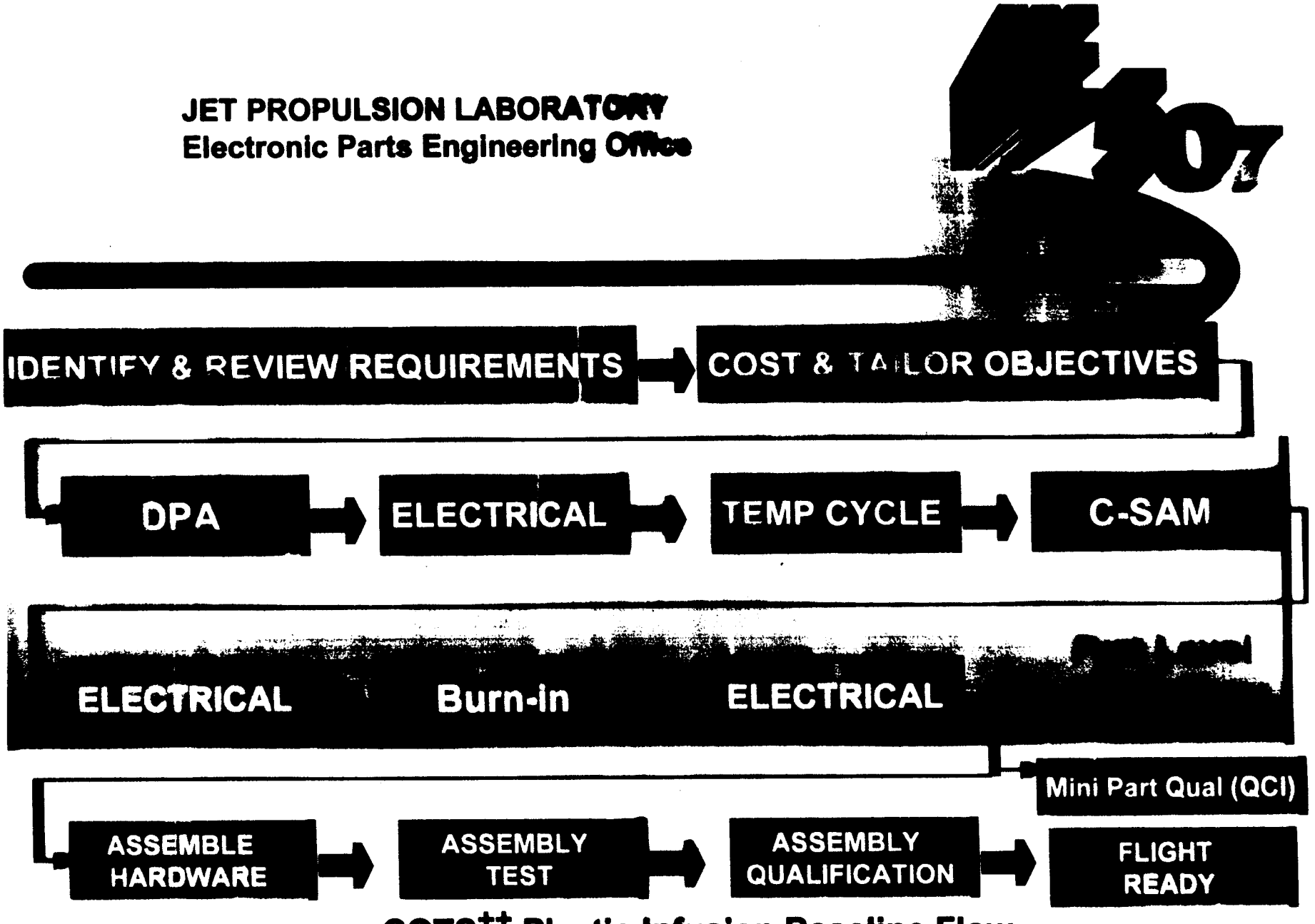

COTS^{++} Plastic Infusion Baseline Flow (Tailored for MARS01 application/mission requirements)

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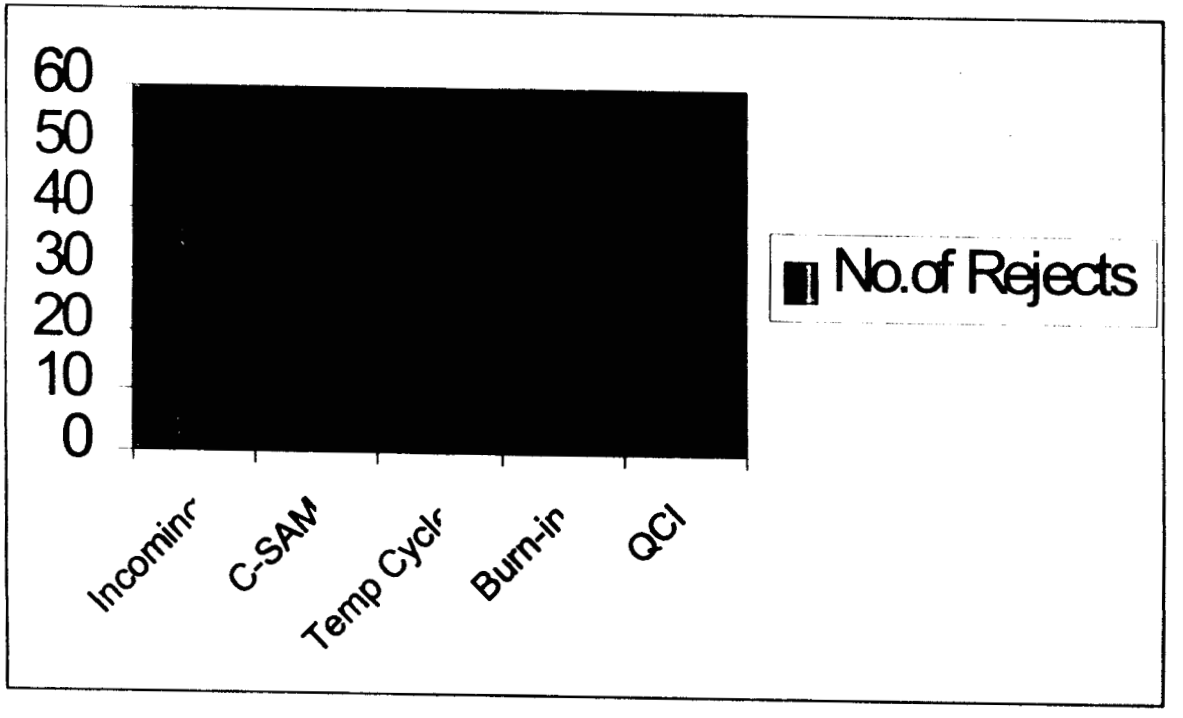
COTS++ Upscreening Results



Incoming = 0.42%

C-SAM = 24.35%

Temp Cycle = 5.55%

Burn-in = 1.28%

QCI = 0.00%

Total = 31.60% (3 types)

Total = 24.8% (5 types)

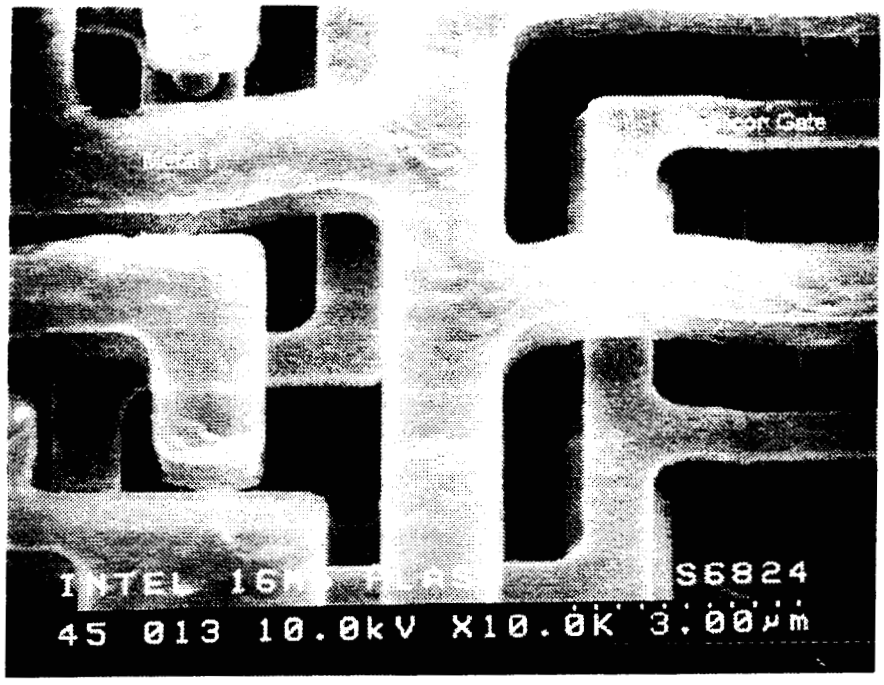


Figure 15. 10kx SEM micrograph showing metallization layer 1 over polysilicon layer 2 gates. Metal layer 1 step coverage was found to be excellent.

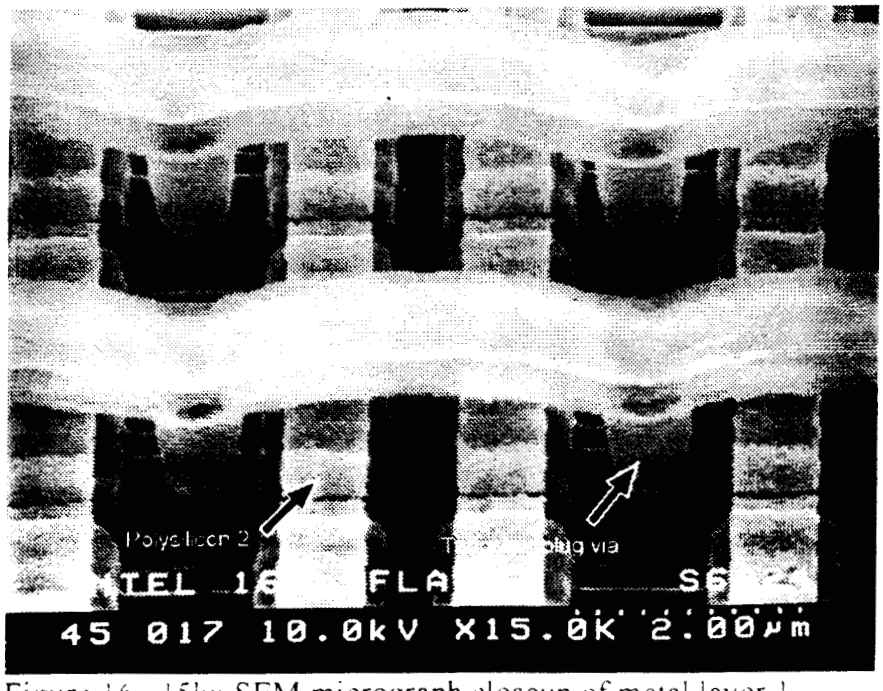


Figure 16. 15kx SEM micrograph closeup of metal layer 1 connections to tungsten plug vias within the memory array. Metal layer 1 is a multilayered structure of aluminum sandwiched between Ti/W layers. Nominal metal 1 thickness was measured to be 0.5 microns.

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Infusion Methods to Insure Low Risk COTS in Critical Sp... ...ations

Guidelines

15 yr mission:	Full Qual/Upscreen	
10 yr mission:	Full Qual/Upscreen	
5 yr mission:	Full Qual/Upscreen	
1 yr mission:	Mini Upscreen/Qual	